CLAIMS

What is claimed is:

1. A method of forming a shallow trench isolation (STI) structure comprising the steps of:

providing a semiconductor substrate;

forming a trench in the semiconductor substrate;

forming one or more liner layers to line the trench;

forming one or more trench filling material layers with stress released material; and

removing excess trench filling material above the trench level.

2. The method of claim 1, further comprising forming at least one patterned hardmask layer selected from the group consisting of silicon nitride and silicon oxynitride over said substrate.

3. The method of claim 1, wherein the semiconductor substrate comprises material selected from the group consisting of silicon, silicon germanium, and gallium arsenide.

4. The method of claim 1, wherein the one or more liner layers are formed according to a method selected from the group consisting of thermal oxidation, LPCVD, and ALCVD.

5. The method of claim 1, wherein chemical reactants to form the one or more liner layers are selected from the group consisting of O_2, SiH_4, NH_3, and N_2O.

6. The method of claim 1, further comprising the step of treating the one or more liner layers with nitrogen (N_2) following the step of forming one or more liner layers according to a treatment selected from the group consisting of a plasma treatment, a thermal anneal, and an implant process in an ambient consisting essentially of nitrogen (N_2) and is.

7. The method of claim 1, wherein the step of forming one or more trench filling material layers comprises a process selected from the group consisting of SACVD, APCVD, HDP-CVD, and spin-coating.

8. The method of claim 9, wherein the process of spin coating comprises forming a spin-on-glass (SOG) comprising a precursor selected from the group consisting of organic and inorganic mixtures for forming cross-linked silicon oxide containing structures.

9. The method of claim 10, wherein the precursor comprises a material selected from the group consisting of siloxanes, silanes, and polysesilquioxanes.

10. The method of claim 9, wherein the SACVD, APCVD, and HDP-CVD processes are carried out comprising chemical reactants selected from the group consisting of TEOS and O_3.

11. The method of claim 9, wherein the SACVD, APCVD, and HDP-CVD processes are carried out comprising chemical reactants selected from the group consisting of SiH_4 and O_2.

12. The method of claim 1, further comprising an intermediate thermal annealing step following formation of trench filling material layers.

13. The method of claim 1, wherein the step of carrying out at least one thermal annealing step is carried out in an ambient selected from the group consisting of O_2 and N_2.

14. The method of claim 1, wherein the step of etching a trench comprises forming a trench comprising sidewalls having an angle with respect to a plane parallel to the substrate major surface of between about 80 degrees and about 89 degrees.

15. The method of claim 1, wherein the step of etching a trench comprises forming a trench comprising rounded top and/or bottom corners.

16. A shallow trench isolation (STI) structure with reduced stress to improve charge mobility comprising:

a semiconductor substrate;

a trench formed through a thickness of the semiconductor substrate;

one or more liner material layers lining the trench;

one or more trench filling material layers comprising silicon dioxide substantially free of stress in a direction substantially parallel or perpendicular to the semiconductor substrate major surface.

17. The STI structure of claim 19, wherein the trench comprises sidewalls having an angle with respect to a plane parallel to the substrate major surface of between about 80 degrees and about 89 degrees.

18. The STI structure of claim 19, wherein the trench comprises rounded top and/or bottom corners.

19. The STI structure of claim 19, wherein the one or more trench filling material layers comprises a portion that extends above the semiconductor substrate surface.

20. The STI structure of claim 22, wherein the portion comprises an inward edge portion extending higher above the substrate surface compared to an outward edge portion.

21. The STI structure of claim 19, wherein the one or more trench filling material layers is selected from the group consisting of organic spin on glass (SOG), inorganic SOG, and undoped silicate glass (USG).

22. The STI structure of claim 19, wherein the one or more trench filling material layers is selected from the group consisting of siloxanes, silicates, and polysesilquioxanes.

23. The STI structure of claim 24, wherein the one or more trench filling material layers comprises a lowermost SOG layer selected from the group consisting of organic and inorganic SOG layers, and an uppermost USG layer.

24. The STI structure of claim 24, wherein the one or more trench filling material layers comprises a lowermost USG layer, an intervening SOG layer selected from the group consisting of organic and inorganic SOG layers, and an uppermost USG layer.

25. The STI structure of claim 24, wherein the one or more trench filling material layers comprises a plurality of USG layers.

26. The STI structure of claim 24, wherein the one or more trench filling material layers comprises a plurality of SOG layers selected from the group consisting of inorganic SOG layers and organic SOG layers.

27. The STI structure of claim 24, wherein the one or more trench filling material layers comprises an uppermost SOG layer selected from the group consisting of inorganic SOG layers and organic SOG layers.

28. The STI structure of claim 19, wherein the one or more liner material layers is formed of a SiO_2/SiN stack

29. The method of claim 19, wherein the one or more liner material layers is formed of a SiO_2/SiON stack.

30. The method of claim 19, wherein the one or more liner material layers is formed of a SiO_2/SiN/SiON stack.

31. The method of claim 19, wherein the one or more liner material layers is formed of one of a SiN/SiON and SiON/SiN stack.